REMARKS

Objection to Claim 5

Claim 5 was objected to under 37 CFR § 1.75(c) as being of improper dependent form for failing to further limit the subject matter of a previous claim.

In response, the applicants have amended claim 5, with the terminology used in the specification on page 4, lines 20-21. It is submitted that the objection to claim 5 has been addressed by the amendment. Therefore, the applicants respectfully request that the objection to claim 5 be withdrawn.

Rejection under 35 U.S.C. § 112, second paragraph, with respect to Claim 4

Claim 4 has been rejected under 35 U.S.C. § 112, second paragraph.

In response, the applicants have amended claim 4 in the manner suggested in the Office Action. Accordingly, withdrawal of the rejection under 35 U.S.C. § 112, second paragraph, is hereby respectfully requested.

Rejection under 35 U. S. C. § 102(b) with respect to claims 1-8

Claims 1-8 have been rejected under 35 U. S.C. § 102(b). The Patent Office has contended that these claims are anticipated by O'Neill (U.S. Patent No. 5,131,978). It is respectfully submitted that this rejection should be withdrawn for the following reasons.

O'Neill teaches low temperature, single side, multiple step etching process for fabrication of small and large structures, where on a planar wafer portion 10, a first masking layer 30, 30' is applied and then a second or protective layer of masking material 32, 32' is applied. After full pattern opening 12, a third masking layer 38, 38' is used to form cavity 20, channel 16, with the layers 30' and 32' covering the bottom opening of the cavity 20 until layers 30' and 32' are subsequently removed. This is very different than that which is being disclosed and claimed by the applicants.

For example, in O'Neill there is no teaching or suggestion to divide the surface of the

wafer into positive areas and negative areas prior to the wet chemical etching process, as disclosed and claimed by the applicants.

Similarly, in O'Neill there is no teaching and/or disclosure to provide the negative areas with a passivation layer to protect the negative areas from the subsequent wet chemical etching process, as disclosed and claimed by the applicants.

In fact, O'Neill teaches away from applicants' invention when in column 4, lines 39-59, he states that on a planar wafer portion 10 "a first masking layer 30 is applied", and that "A second or protective layer of masking material 32 is formed on the silicon nitride layer masking layer 30." On the other hand, the applicants have positive areas and negative areas defined prior to any etching.

Similarly, O'Neill teaches away from applicants' invention when in column 5, lines 14-15, he states that "The second masking layer 32 is etched with an appropriate wet etchant". Even at this "wet etching" step O'Neill still has not defined his positive and negative areas, as disclosed and claimed by the applicants.

Additionally, O'Neill teaches away from applicants' invention when in column 5, lines 27-31, he teaches that "a third masking layer 38 ... is formed over the remaining portions of the first and second masking layers and over the exposed surfaces of the wafer formed by the opening 12." On the other hand, the applicants are disclosing and claiming that after dividing the positive areas and the negative areas a passivation layer is provided to "protect the negative areas from the subsequent wet chemical etching process".

In fact, "the positive areas 20" in O'Neill, as pointed out by the examiner, appear only after a portion of the third masking layer 38 is removed.

Additionally, "the positive areas 20" in O'Neill, as pointed out by the examiner, has at least one first layer 30, at least one second layer 32, and then at least one third layer 38 over it, prior to the creation of the "the positive areas 20" in O'Neill, as pointed out by the examiner.

Furthermore, with regard to edge protection of the wafer using Applicants' negative technique, a further difference between O'Neill and the Applicants is that even when removal of resist from the edge of the wafer is missing (which is, however, not standard in IC processing) in mass production using procedures customary up till now (and described in the art) "no silicon wafers are etched with potassium hydroxide (KOH)", without undergoing slight etching at the wafer edge. In a positive technique, the edge of the wafer has to be protected by resist which is extremely susceptible to damage. With the Applicants' method one obtains the "perfect" edge protection even with the standard semiconductor photo technique.

For the preceding reasons, withdrawal of the rejection under 35 U.S.C. § 102(b) with respect to Claims 1-8, is hereby respectfully requested.

Rejection under 35 U. S. C. § 102(e) with respect to claims 1-3 and 5-8

Claims 1-3 and 5-8 have been rejected under 35 U. S.C. § 102(e). The Patent Office has contended that these claims are anticipated by Burns et al. (U.S. Patent No. 5,738,757). It is respectfully submitted that this rejection should be withdrawn for the following reasons.

Burns is directed to a planar masking for multi-depth silicon etching, where a planar silicon wafer 10 has a first layer of silicon dioxide 12, a first layer of silicon nitride 14, a second silicon dioxide layer 16, and a second silicon nitride layer 18. This arrangement is very different than what is being disclosed and claimed by the applicants.

For example, in Burns there is no teaching or suggestion to divide the surface of the wafer into positive areas and negative areas prior to the wet chemical etching process, as disclosed and claimed by the applicants.

Similarly, in Burns there is no teaching or suggestion for providing the negative areas with a passivation layer to protect the negative areas from the subsequent wet chemical etching process, as disclosed and claimed by the applicants.

In fact, Burns teaches away from applicants' invention when in column 5, lines 24-31, he clearly states that "a layer of silicon dioxide 12 is grown on a planar silicon wafer 10, after which the three layers 14, 16 and 18 are deposited ... Thus, four layers of alternating masking material are provided for the desired three etch depths." On the other hand, the applicants have positive areas and negative areas defined prior to any etching.

Similarly, Burns teaches away from applicants' invention when in column 5, lines 33-36, he clearly states that "silicon nitride layer 18 and underlying portions of silicon dioxide layer 16 are etched in turn in nitride and oxide etchants". Even at this two "etching" step Burns still has not defined his positive and negative areas, as disclosed and claimed by the applicants.

Additionally, Burns teaches away from applicants' invention when in column 5, lines 38-44, he clearly teaches that "the exposed portions of silicon nitride layer 14 are removed by using a nitride etchant". On the other hand, the applicants are disclosing and claiming that after dividing the positive areas and the negative areas a passivation layer is provided to "protect the negative areas from the subsequent wet chemical etching process".

In fact, "the positive areas" in Burns, as pointed out by the examiner, appear only after a portion of the fourth masking layer 12, is removed.

Additionally, "the positive areas" in Burns, as pointed out by the examiner, has at least one first layer 12, at least one second layer 14, at least one third layer 16, and at least one fourth layer 18 over it, prior to the creation of "the positive areas" in Burns, as pointed out by the examiner.

Furthermore, with regard to edge protection of the wafer using Applicants' negative technique, a further difference between Burns and the Applicants is that even when removal of resist from the edge of the wafer is missing (which is, however, not standard in IC processing) in mass production using procedures customary up till now (and described in the art) "no silicon wafers are etched with potassium hydroxide (KOH)", without undergoing slight etching at the wafer edge. In a positive technique, the edge of the wafer has to be protected by resist which is extremely susceptible to damage. With the Applicants' method one obtains the "perfect" edge protection even with the standard semiconductor photo technique.

For the preceding reasons, withdrawal of the rejection under 35 U.S.C. § 102(e) with respect to Claims 1-3 and 5-8, is hereby respectfully requested.

Rejection under 35 U.S. C. § 103 (a) with respect to claims 1-3 and 5-9

Claims 1-3 and 5-9 have been rejected under 35 U.S.C. § 103(a) over Burns et al. (U.S. Patent No. 5,738,757). It is respectfully submitted that this rejection should be withdrawn for the following reasons.

The earlier discussion with reference to Burns is incorporated herein by reference.

As the applicants have pointed out, Burns teaches away from applicants' invention, and therefore, even if the Patent Office takes official notice of the "LOCOS process", there is no showing why a person skilled in the art would combine the "LOCOS process" with a reference that teaches away from applicants' invention.

Furthermore, it would not be obvious to one skilled in the art to utilize a reference that teaches away from applicants' invention.

For the reasons discussed above with respect to the rejection of claims 1-3 and 5-9, withdrawal of the rejection under 35 U.S.C. § 103 (a) with respect to claims 1-3 and 5-9, is hereby respectfully requested.

Conclusion

It is believed that this application is now in condition for allowance and applicants respectfully request such action.

Respectfully Submitted,

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